

What is claimed:

1 1. A method for manufacturing a semiconductor device, the semiconductor
2 device having a DRAM including a cell capacitor formed in a DRAM region of a
3 semiconductor substrate, and a capacitor element formed in an analog element region of the
4 semiconductor substrate, the method comprising the steps of:

- 5 (a) simultaneously forming a storage node of the cell capacitor and a lower electrode
6 of the capacitor element;
7 (b) simultaneously forming a dielectric layer of the cell capacitor and a dielectric
8 layer of the capacitor element; and
9 (c) simultaneously forming a cell plate of the cell capacitor and an upper electrode of
10 the capacitor element.

1 2. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising, before the step (a), the step of simultaneously forming
3 a word line that is a component of the DRAM and
4 a connection layer that is located in a common layer of the word line and that
5 electrically connects the lower electrode to another element in the semiconductor device.

1 3. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising the step of:
3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,
5 wherein the step (d) is carried out simultaneously with step (c), and
6 wherein a number of ion-implantations of impurity in a region where the first
7 resistance element is to be formed is greater than a number of ion-implantations of impurity
8 in a region where the second resistance element is to be formed so that a resistance value of
9 the first resistance element is lower than a resistance value of the second resistance element.

1 4. A method for manufacturing a semiconductor device according to claim 2,
2 further comprising the step of:

3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,

5 wherein the step (d) is carried out simultaneously with step (c), and

6 wherein a number of ion-implantations of impurity in a region where the first
7 resistance element is to be formed is greater than a number of ion-implantations of impurity
8 in a region where the second resistance element is to be formed so that a resistance value of
9 the first resistance element is lower than a resistance value of the second resistance element.

1 5. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising the step of:

3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,

5 wherein the step (d) is carried out simultaneously with step (c), and

6 wherein an impurity is diffused in a region where the first resistance element is to be
7 formed so that a resistance value of the first resistance element is lower than a resistance
8 value of the second resistance element.

1 6. A method for manufacturing a semiconductor device according to claim 2,
2 further comprising the step of:

3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,

5 wherein the step (d) is carried simultaneously with step (c), and

6 wherein an impurity is diffused in a region where the first resistance element is to be
7 formed so that a resistance value of the first resistance element is lower than a resistance
8 value of the second resistance element.

1 7. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising the step of:

3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,

5 wherein the step (d) carried out simultaneously with step (c), and

6 wherein a silicide layer is formed in a region where the first resistance element is to
7 be formed so that a resistance value of the first resistance element is lower than a resistance
8 value of the second resistance element.

1 8. A method for manufacturing a semiconductor device according to claim 2,
2 further comprising the step of:

3 (d) forming a first resistance element and a second resistance element in the analog
4 element region,

5 wherein the step (d) is carried out simultaneously with step (c), and

6 wherein a silicide layer is formed in a region where the first resistance element is to
7 be formed so that a resistance value of the first resistance element is lower than a resistance
8 value of the second resistance element.

1 9. A semiconductor device having a DRAM including a cell capacitor formed
2 in a DRAM region of a semiconductor substrate, and a capacitor element formed in an
3 analog element region of the semiconductor substrate, the semiconductor device
4 comprising:

5 an interlayer dielectric layer and an embedded connection layer,

6 wherein the interlayer dielectric layer is located between the semiconductor substrate
7 and the capacitor element,

8 the embedded connection layer is used to electrically connect a lower electrode of
9 the capacitor element to another semiconductor element,

10 the embedded connection layer is located at a connection hole formed in the
11 interlayer dielectric layer, and

12 one end section of the embedded connection layer connects to the lower electrode at
13 a bottom surface of the lower electrode.

1 10. A semiconductor device according to claim 9, further comprising
2 a connection layer connected to a second end section of the embedded connection
3 layer,
4 wherein the connection layer is used to electrically connect the lower electrode to
5 another semiconductor element, and
6 the connection layer is located in a common layer of a word line that is a component
7 of the DRAM.

1 11. A semiconductor device according to claim 10, further comprising
2 an additional capacitor element,
3 wherein the additional capacitor element is located in the analog element region, and
4 the capacitor element and the additional capacitor element are serially connected to
5 each other by the embedded connection layer and the connection layer.

1 12. A semiconductor device according to claim 9 further comprising a first
2 resistance element and a second resistance element,
3 wherein the first resistance element and the second resistance element are located in
4 the analog element region, and
5 an impurity concentration of the first resistance element is higher than an impurity
6 concentration of the second resistance element so that a resistance value of the first
7 resistance element is lower than a resistance value of the second resistance element.

1 13. A semiconductor device according to claim 9, further comprising a first
2 resistance element and a second resistance element,
3 wherein the first resistance element and the second resistance element are located in
4 the analog element region, and
5 the first resistance element includes a silicide layer so that a resistance value of the
6 first resistance element is lower than a resistance value of the second resistance element.

1 14. A semiconductor device according to claim 9, wherein a thickness of a
2 dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of
3 the cell capacitor.

1 15. A method for manufacturing a semiconductor device, the semiconductor
2 device having a DRAM including a cell capacitor formed in a DRAM region of a
3 semiconductor substrate, and a capacitor element formed in an analog element region of the
4 semiconductor substrate, the method comprising:
5 forming a first conducting layer and etching a portion of the first conducting layer to
6 form a storage node of the cell capacitor and a lower electrode of the capacitor element;
7 forming a dielectric layer and etching a portion of the dielectric layer to form a
8 dielectric layer region of the cell capacitor and a dielectric layer region of the capacitor
9 element; and
10 forming a second conducting layer and etching a portion of the second conducting
11 layer to form a cell plate of the cell capacitor and an upper electrode of the capacitor
12 element.

1 16. A method according to claim 15, further comprising, prior to forming the
2 storage node of the cell capacitor and the lower electrode of the capacitor element,
3 form an additional conducting layer and etching the additional conducting layer to
4 form a word line that is a component of the DRAM and to form a connection layer that is
5 located in a common layer of the word line and that is configured to electrically connect the
6 lower electrode to another element in the semiconductor device.

1 17. A method for manufacturing a semiconductor device according to claim 15,
2 wherein the etching a portion of the second conducting layer also forms a first resistance
3 element and a second resistance element in the analog element region, and wherein the first
4 resistance element and second resistance element are formed with a resistance value of the
5 first resistance element being lower than that of the second resistance element.

1 18. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising the step of:
3 (d) forming a first resistance element and a second resistance element in the analog
4 element region, wherein the step (d) is carried out simultaneously with step (c), and wherein
5 an amount of impurity ion-implanted in a region where the first resistance element is to be
6 formed is greater than an amount of impurity ion-implanted in a region where the second
7 resistance element is to be formed so that a resistance value of the first resistance element is
8 lower than a resistance value of the second resistance element.

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